Parametric Analysis of an AlScN based Ferroelectric Capacitor Model in a Ferroelectric Memory Bitcell

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This paper demonstrates the design and simulation of a 1-transistor-1-capacitor (1T-1C) ferroelectric random access memory (FeRAM) bitcell. The emergence of aluminum scandium nitride (AlScN) as a ferroelectric material and its compatibility with the silicon carbide (SiC) CMOS process has enabled the design of non-volatile memory (NVM) solutions suitable for harsh environment applications [1]. This requires the development of compact models for the ferroelectric capacitor (FeCap) to understand the functionality of an integrated memory. This work focuses on the demonstration of FeRAM bitcell using FeCap model based on $Al_{0.7}Sc_{0.3}N$ in Cadence Virtuoso [1] [2]. Additionally, this study provides insight on the critical parameters including the ferroelectric thickness and remanent polarization (P_r) relationship with coercive electric fields (E_c) to achieve the required ferroelectric switching. A 1T-1C bitcell is designed and simulated for varying thickness of an $Al_{0.7}Sc_{0.3}N$ ferroelectric material (20 nm - 50 nm) corresponding to a coercive voltage (V_c) ranging from 8V to 20V for an E_c of 4 MV/cm. Fig. 1 shows the timing diagrams for a write operation that starts from the FeCap pristine state and is subsequently written into 1,

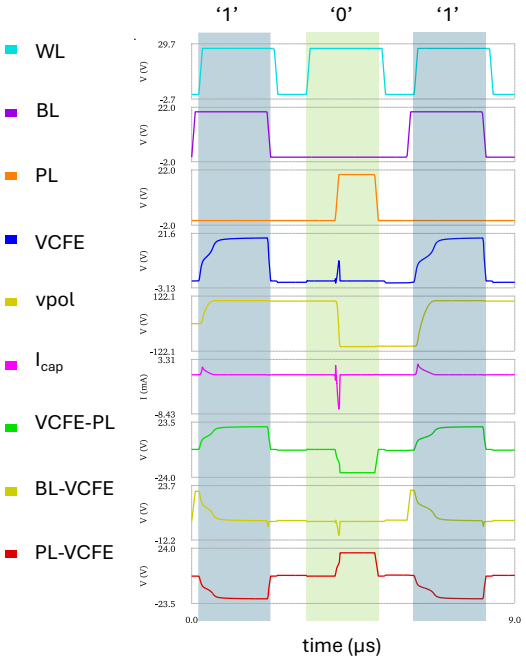

Fig. 1. Write 1-0-1 operation in a FeRAM bitcell for an $Al_{0.7}Sc_{0.3}N$ thickness of 25 nm and VDD= 20 V. The changes in ferroelectric polarization states are depicted by virtual polarization charge state vpol waveform where vpol is a positive saturated value for 1-state and negative saturated value for a 0-state.

0 and 1 states. When the bitline (BL) is taken high relative to the plateline (PL). The ferroelectric polarization charge (vpol) transitions to a positive value (a.u.) indicating a 1-state. Reversal of the BL and PL potentials results in vpol transitioning to a negative value (a.u.), thus indicating a 0-state. Positive and negative current (I_{cap}) spikes can also be observed for the corresponding polarization switching for the 1,0,1 write operation as indicated in the sixth signal (pink) trace in Fig. 1. This phenomenon is, however, not evident in Fig. 2, when consecutive '1s' and '0s' are written. Here the I_{cap} spikes can only be observed for the first write '1' or write '0' indicating the switching event. Time dependent voltage traces across the individual transistor and FeCap components are also provided in Fig. 1 and 2 and will be described in detail in the paper. Furthermore, this paper also discusses the thin film fabrication limitations for $Al_{0.7}Sc_{0.3}N$ and the availability of high voltage SiC CMOS process to cater to the V_c requirements corresponding to this thin film ferroelectric material.

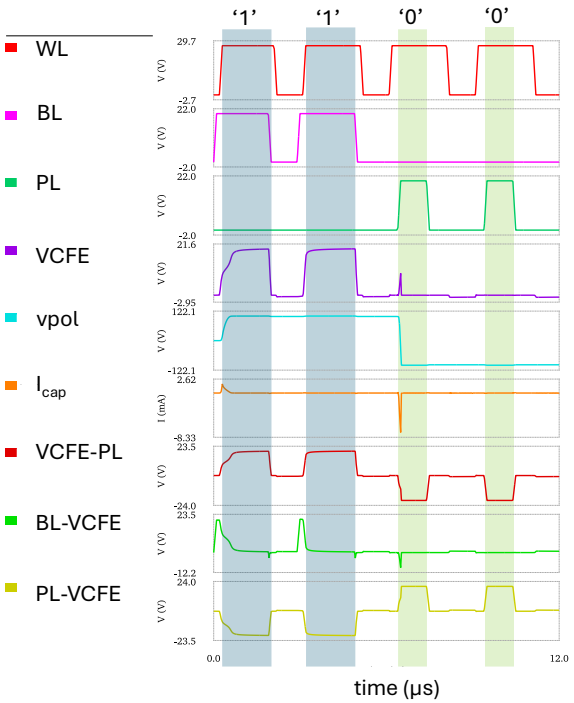

Fig. 2. Write 1-1-0-0 operation in a FeRAM bitcell for an $Al_{0.7}Sc_{0.3}N$ thickness of 25 nm and VDD=20 V. For consecutive write '1' and write '0' the vpol is held at a positive saturated value for a 1-state and a negative saturated value for a 0-state.

References

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